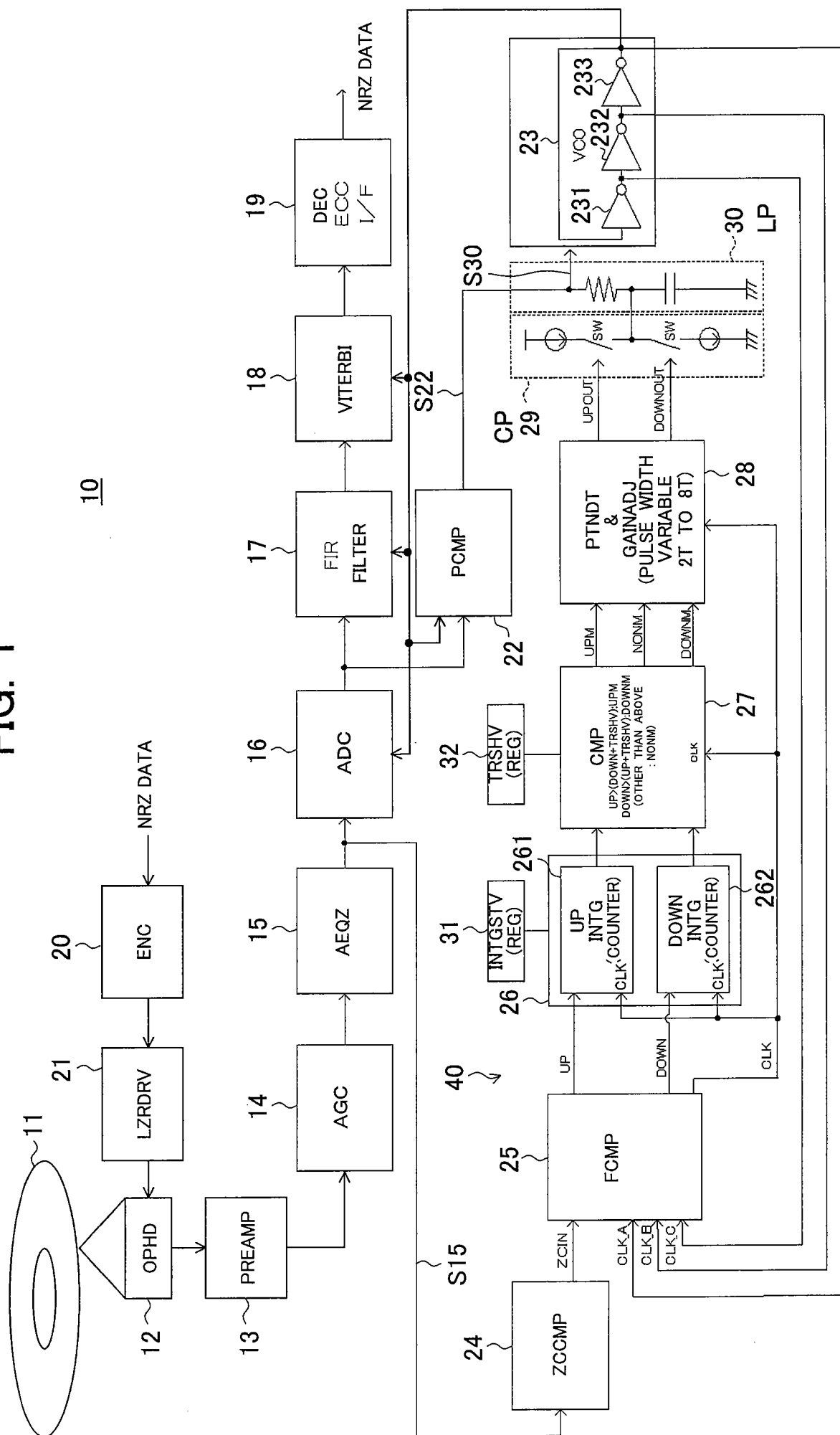


10



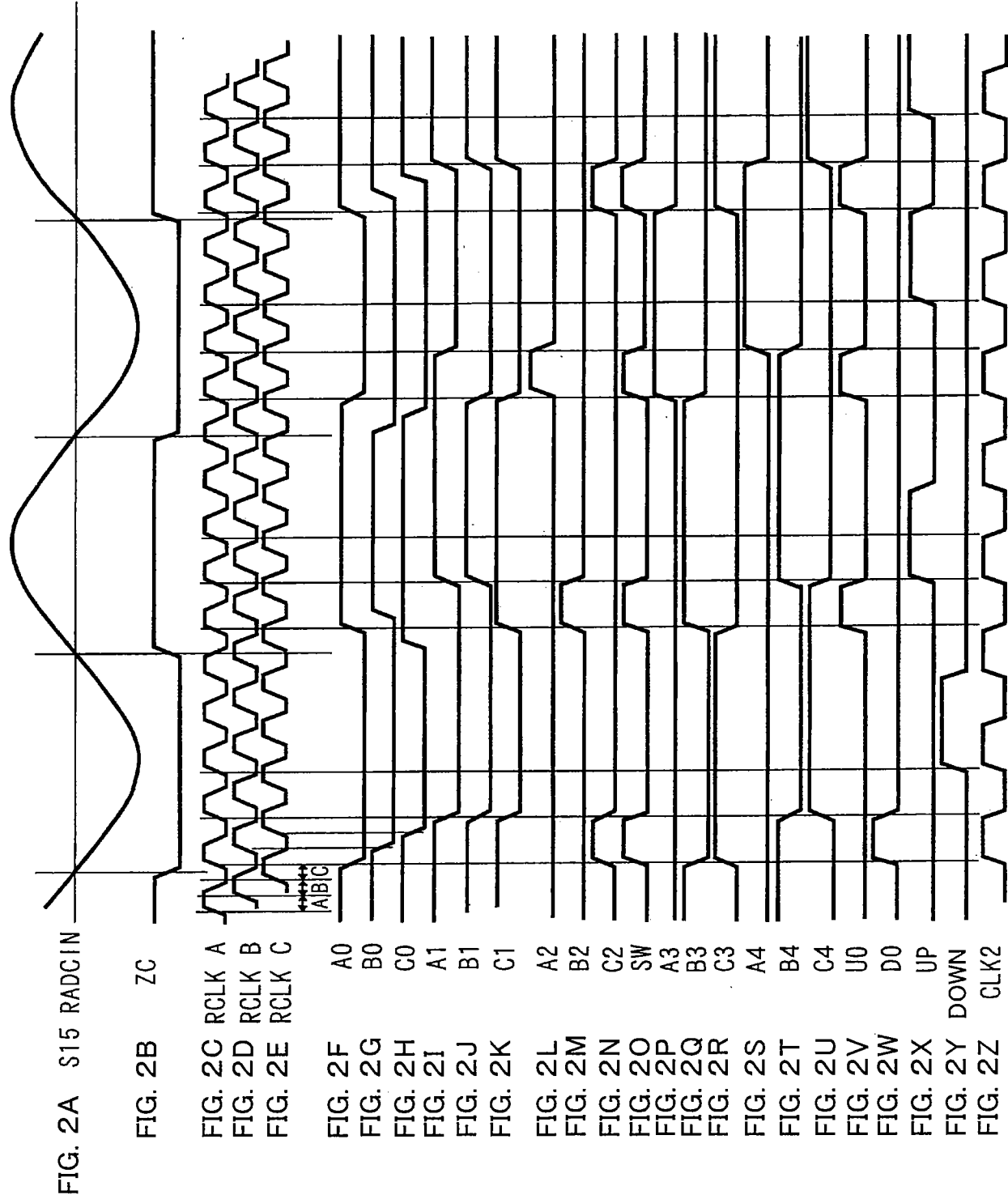


FIG. 3

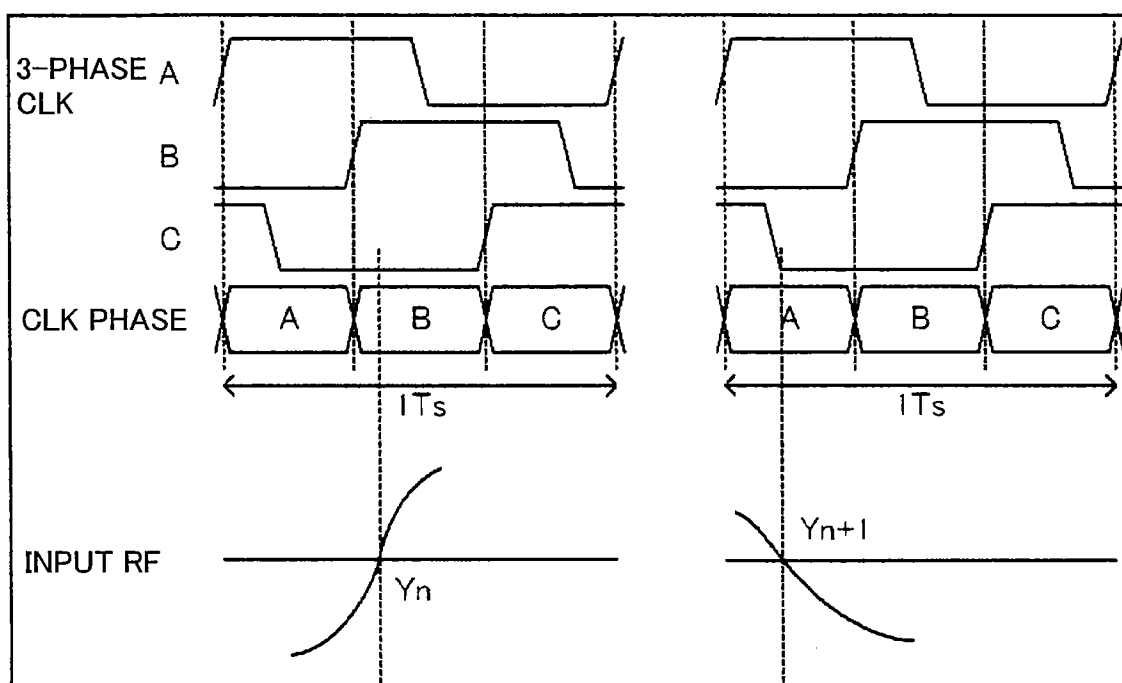


FIG. 4

FREQUENCY COMPARATOR LOGIC

Y_n	Y_{n+1}	UP	DOWN
A	A	0	0
A	B	0	1
A	C	1	0
B	A	1	0
B	B	0	0
B	C	0	1
C	A	0	1
C	B	1	0
C	C	0	0

FIG. 5

25

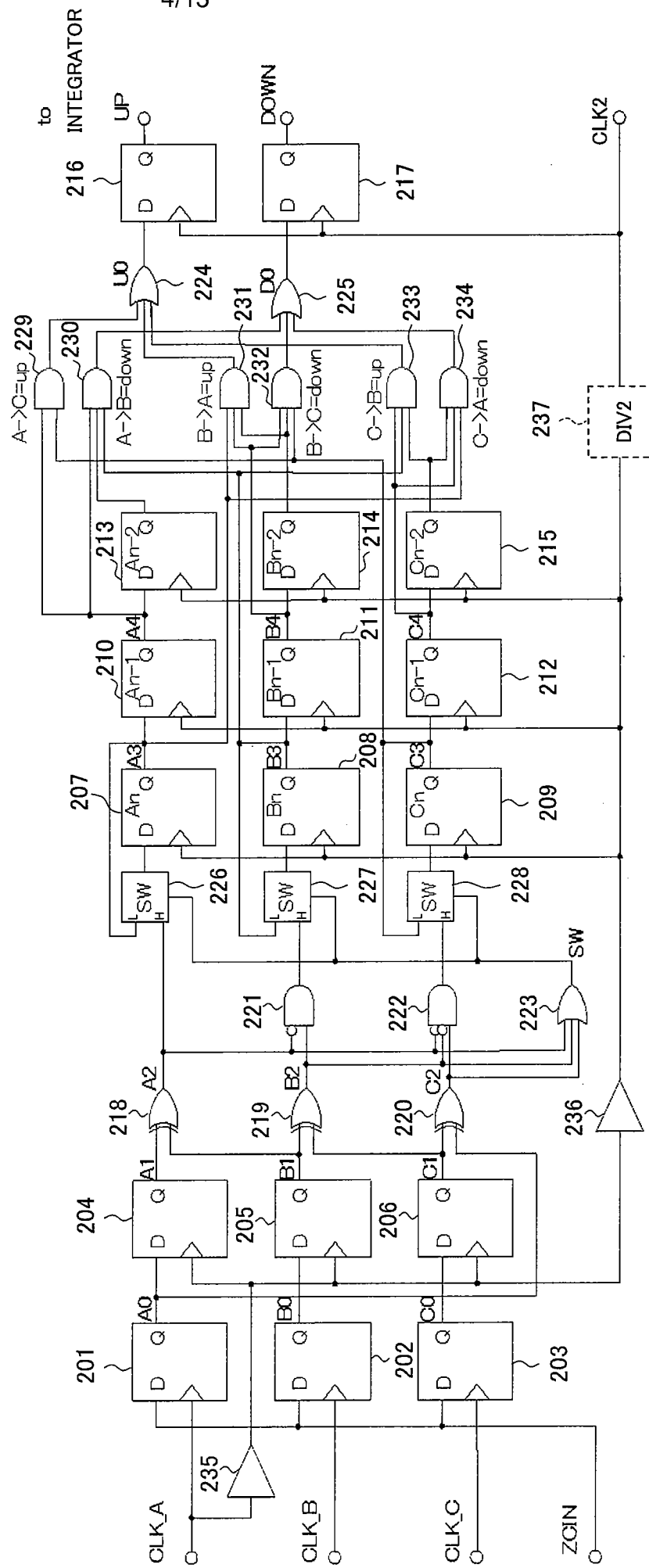


FIG. 6

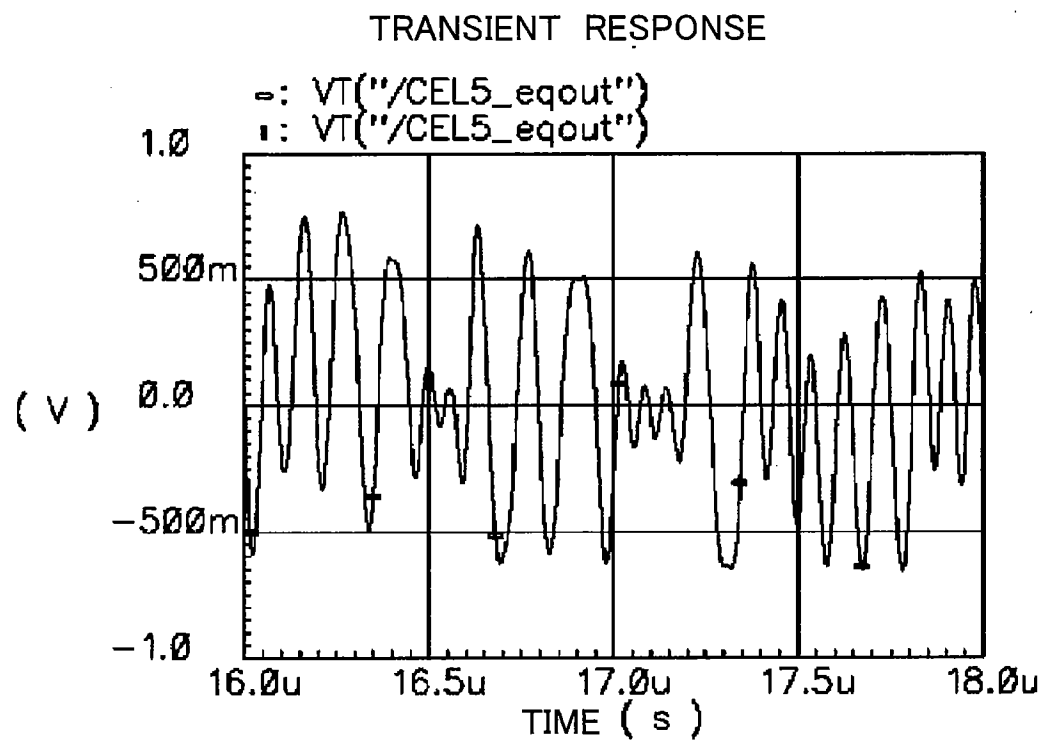


FIG. 7
EXAMPLE OF ZERO CROSS DISTRIBUTION

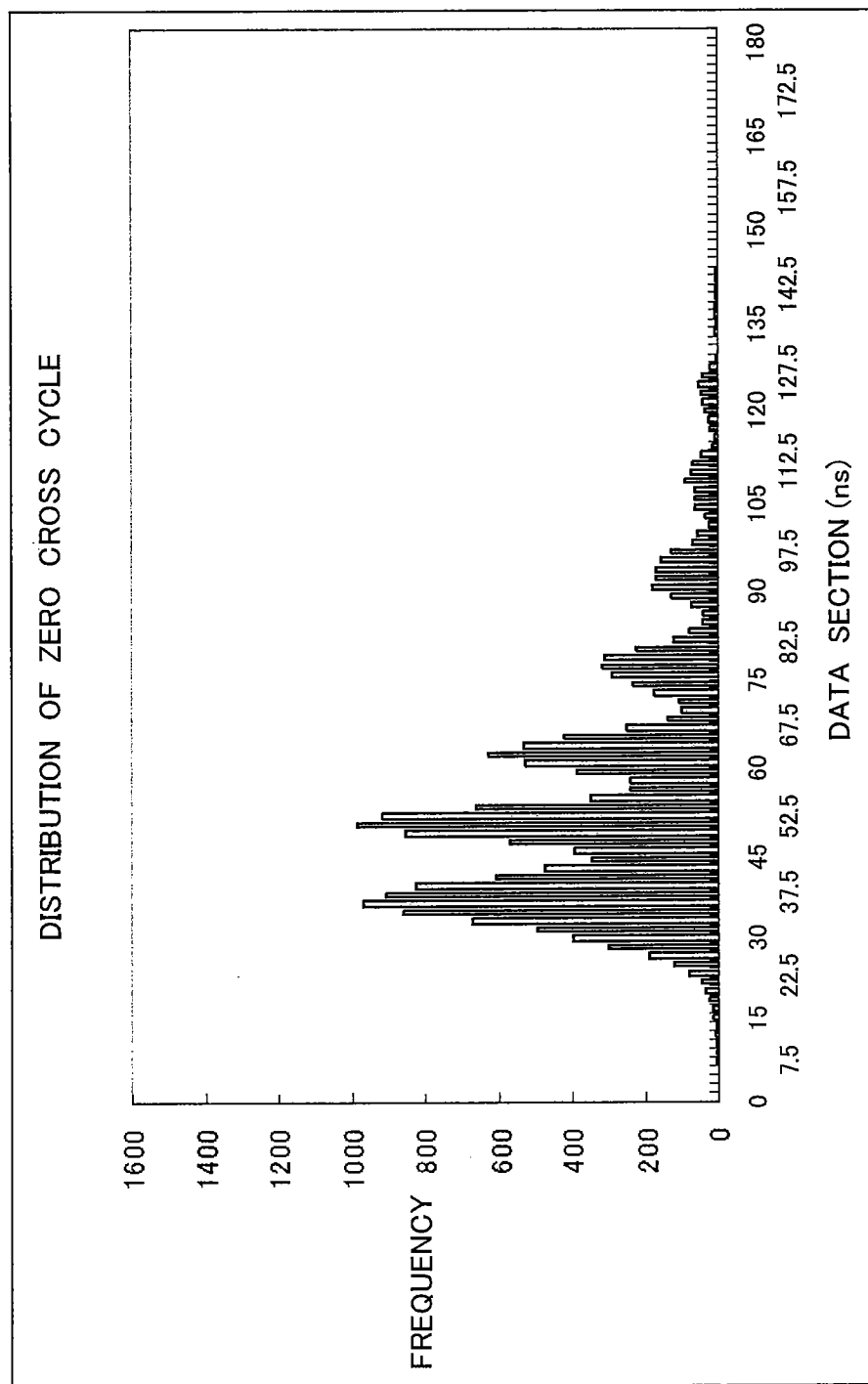
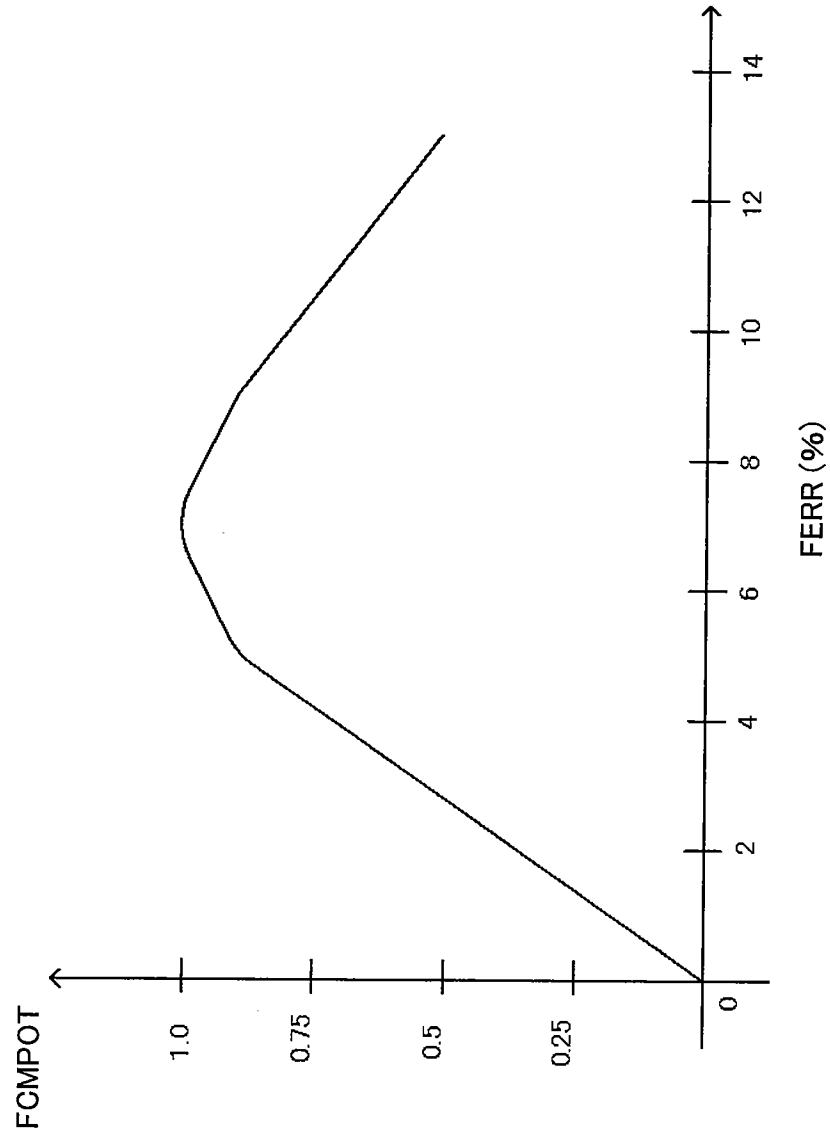


FIG. 8
CASE OF BD ROM (THEORETICAL VALUE)



(CASE WHERE INTEGRATION SETTING VALUE = 8, JUDGEMENT THRESHOLD VALUE = 4, UPM IS OUTPUT)

FIG. 9A CLK

FIG. 9B UP

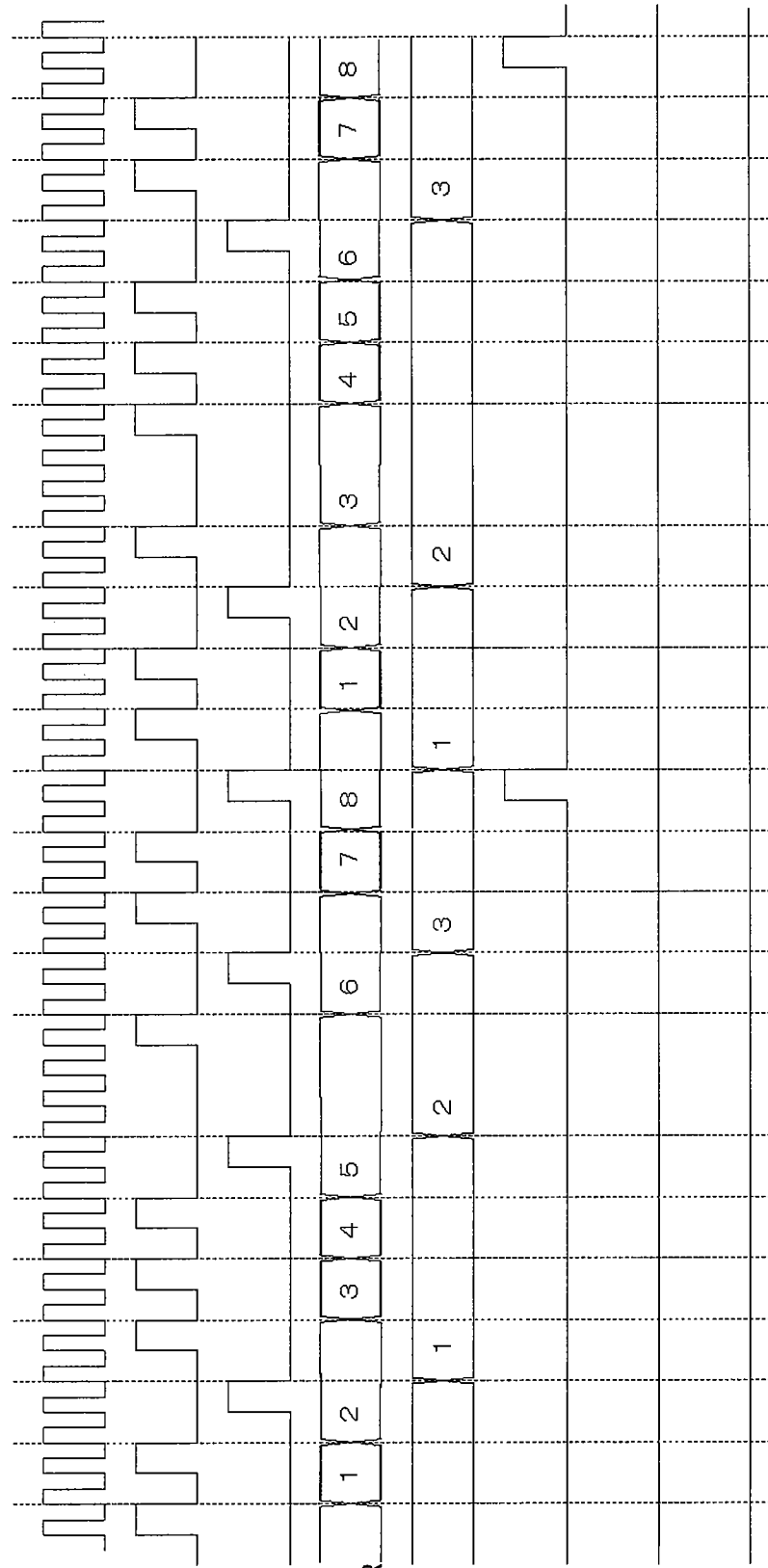
FIG. 9C DOWN

FIG. 9D UP
COUNTERFIG. 9E DOWN
COUNTER

FIG. 9F UPM

FIG. 9G DOWNM

FIG. 9H NONM



(CASE WHERE INTEGRATION SETTING VALUE = 8, JUDGEMENT THRESHOLD VALUE = 4, NONM IS OUTPUT)

FIG. 10A CLK

FIG. 10B UP

FIG. 10C DOWN

FIG. 10D UP
COUNTERFIG. 10E DOWN
COUNTER

FIG. 10F UPM

FIG. 10G DOWNM

FIG. 10H NONM

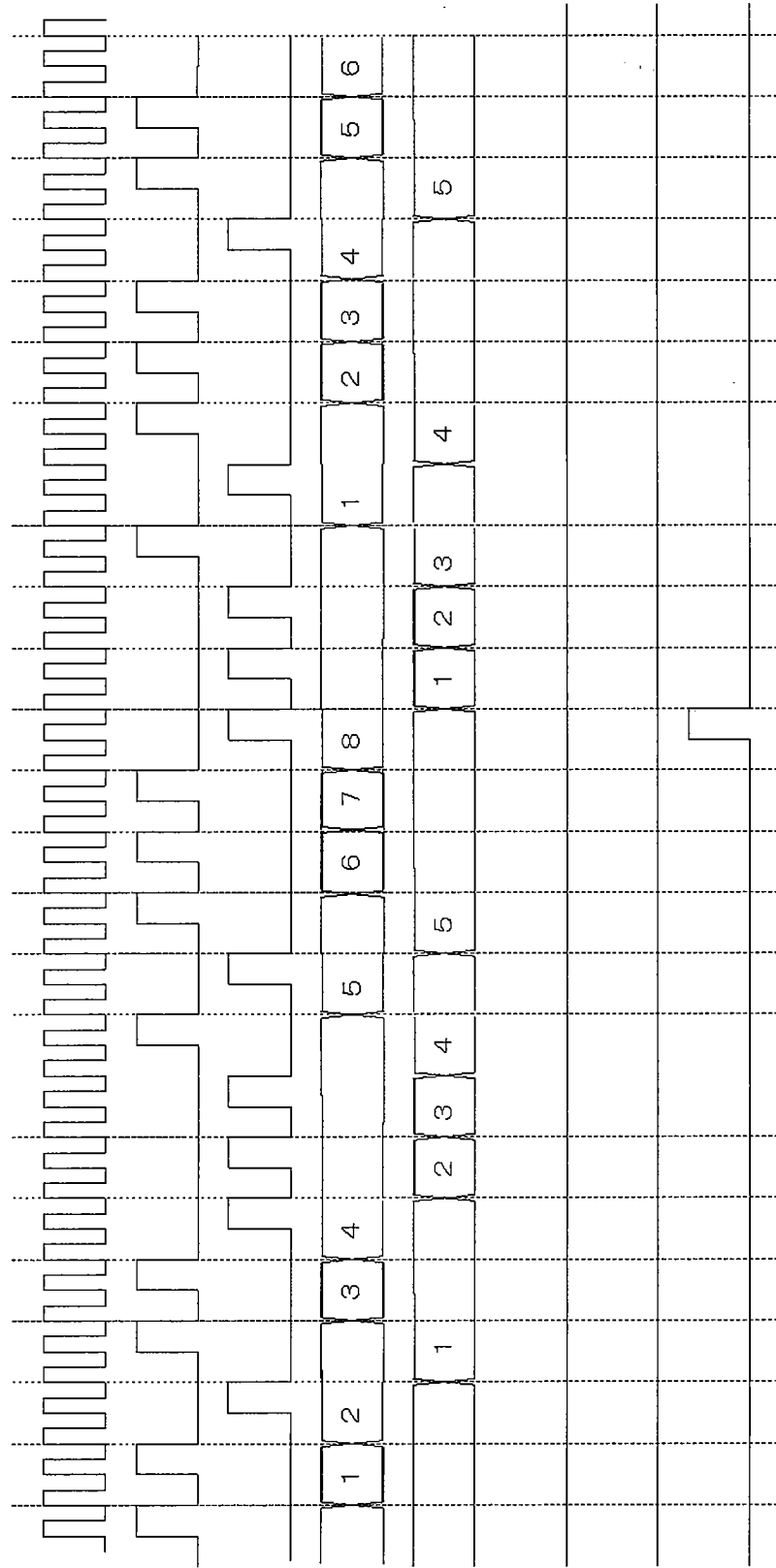


FIG. 11

THREE TIME PREVIOUS COMPARATOR OUTPUT	TWO TIME PREVIOUS COMPARATOR OUTPUT	ONE TIME PREVIOUS COMPARATOR OUTPUT	PRESENT COMPARATOR OUTPUT	OUTPUT		
				OUTPUT	GAIN (PULSE WIDTH)	
OTHER THAN UPM	OTHER THAN UPM	OTHER THAN UPM	UPM	NONE	0	
	EITHER IS UPM			UPOUT	0.25(1T)	
OTHER THAN UPM	OTHER THAN UPM	UPOUT		0.25(1T)		
OTHER THAN UPM	UPM	UPOUT		0.5(2T)		
UPM	UPM	UPOUT		1(4T)		
OTHER THAN DOWNM	OTHER THAN DOWNM	OTHER THAN DOWNM		DOWNM	NONE	0
EITHER IS DOWNM					DOWNOUT	0.25(1T)
OTHER THAN DOWNM	OTHER THAN DOWNM	DOWNOUT	0.25(1T)			
OTHER THAN DOWNM	DOWNM	DOWNOUT	0.5(2T)			
DOWNM	DOWNM	DOWNOUT	1(4T)			
ALL	ALL	ALL	NONM		NONE	0

INITIAL OPERATION OF FREQUENCY LOCK-IN

FIG. 12A

UPM

FIG. 12B

DOWNM

FIG. 12C

NONM

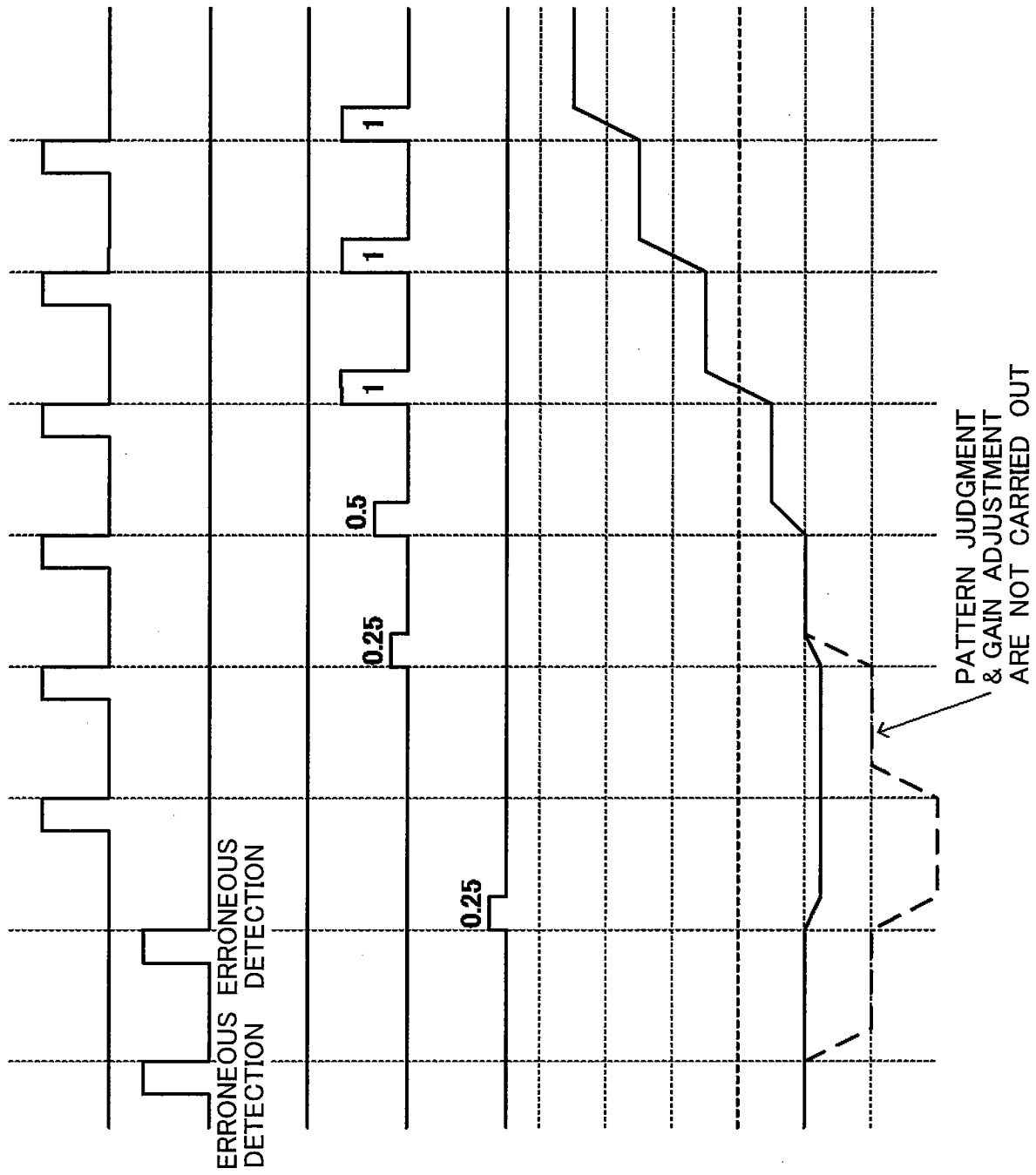
FIG. 12D

UPOUT
GAIN

FIG. 12E

DOWNOUT
GAIN

FIG. 12F

VCO
CONTROL
VOLTAGE

OPERATION AT CONVERGENCE

FIG. 14A

UPM

FIG. 14B

DOWNM

FIG. 14C

NONM

FIG. 14D

UPOUT
GAIN

FIG. 14E

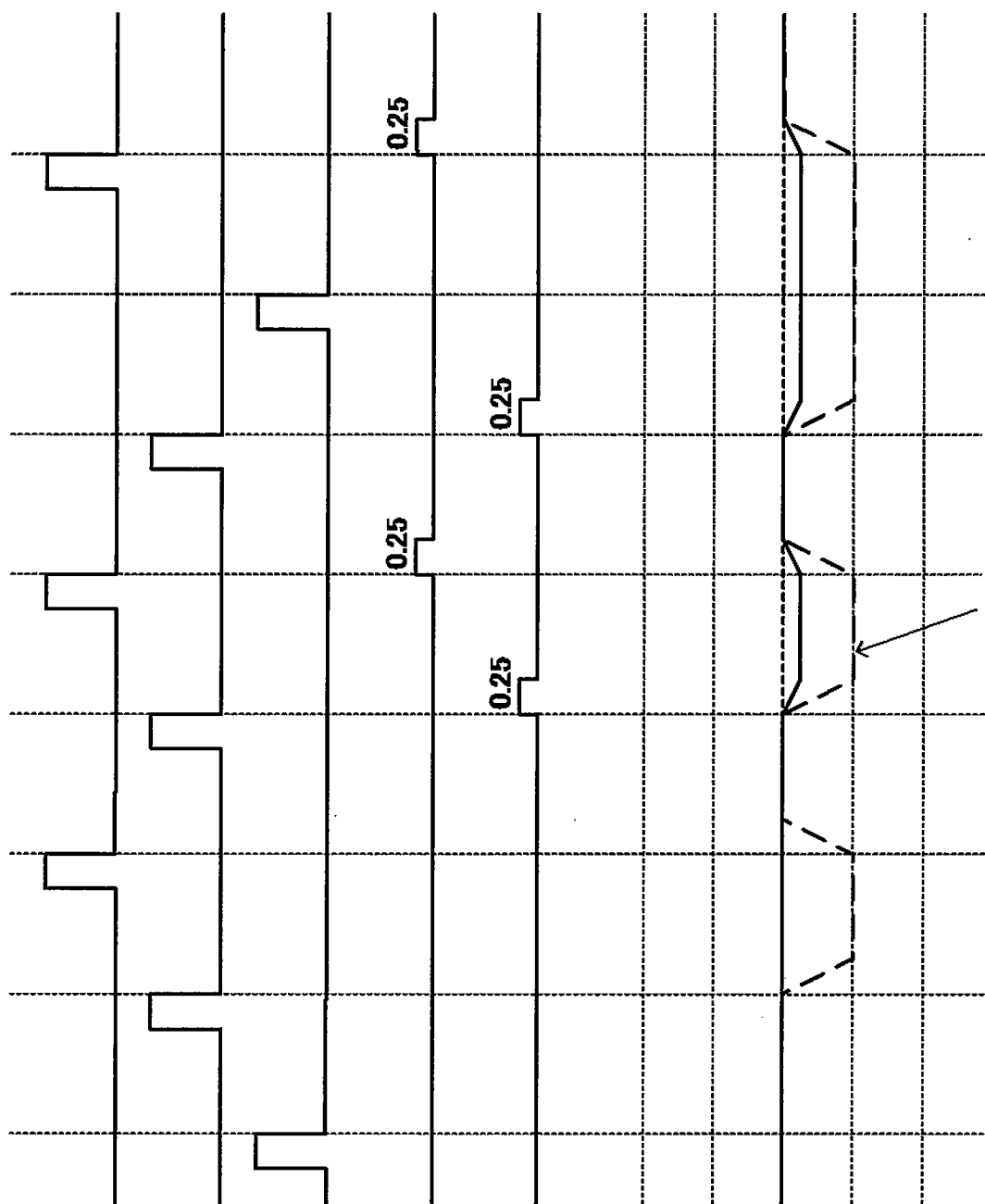
DOWNOUT
GAIN

FIG. 14F

VCO
CONTROL
VOLTAGE